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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,643	11/15/2000	John E. Gavlik	P04762	3643

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EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,643	GAVLIK ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are subject to examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 08, 2005 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 9 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper (US 6,182,238) in view of Johnson et al. (hereinafter Johnson) (US 4,530,051) and further in view of Kaneko et al. (hereinafter Kaneko) (US 5, 127, 096)

6. Cooper and Johnson were cited by the Examiner in a previous Office Action.

Referring to claims 1 and 2,

Cooper teaches the buses to which the microcontroller can be connected such as peripheral component interface (PCI) or special purpose buses, thereby the reference suggests that the microcontroller can be used on a network interface card providing an interface between the network and the PCI bus. (Fig. 1 and col.5, lines 28-33). The reference also discloses microcontroller which is capable of executing multitasking control program (firmware instructions, task initialization and service routines) with first memory (ROM 200) capable of storing multitasking control program including service routines, and second memory (RAM 202) capable of storing plurality of multitasking vectors (operational parameters, task execution flags, task status flags) associated with multitasking control program (firmware instructions, task initialization and service routines). Also the reference teaches the communication taking place between the first memory (ROM 200) and the second memory (RAM 202) (col.3, lines 15-65 and Fig. 2).

Although, Copper teaches, the first memory includes microcontroller firmware instructions, task initialization and service routines, he fails to explicitly teach multitasking control program comprising a main routine and a plurality of subroutines callable by the main routine, and a routine of first memory calling a subroutine and upon encountering a decision point that is not yet capable of being decided, updates the vector with the address of decision point associated with the subroutine and transferring the program execution control back to the main routine.

Johnson teaches the process (main routine) comprising of a collection of procedures (a plurality of subroutines), each performing some subtask of the process. Johnson goes on teaching that the process for the needed data can call these procedures where the data is exchanged via stack (memory data structure) (col.4, lines 60-68 and col.5, lines 1-24). Johnson also teaches that the procedure can be placed into dormant state (a decision point that is not yet capable of being decided) and the status message of the procedure is updated (updating the vector of the subroutine) and then the process can resume another procedure by calling and transitioning to execution state. After the completion of another procedure, the process can come back to the dormant procedure to continue the execution from where it left the procedure. (col. 7, lines 10-68 and col.8, lines 1-28, Figs.) and 5). Johnson also teaches in col. 6, lines 37-41, "Processes communicate with each other via interprocess messages which are placed in message queues such as message queue 240, which contains messages 241, 242, . . . , 243. These queues operate on a first-in, first-out queuing discipline in this example."

Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a network interface card with a microcontroller including multitasking control program comprising the main routine and a plurality of subroutines callable by main routine in the first memory as taught by Johnson and providing multitasking vectors in the second memory associated with the multitasking control program where the status of the subroutines is updated periodically for coming back to check it's progress of execution because if one subroutine fails to terminate the

microcontroller becomes incapable of executing any further instructions as taught by Cooper.

Cooper and Johnson teach the claimed elements except a plurality of subroutines sequentially callable by said main routine and wherein the main routine a after sequentially transferring program execution control to each remaining subroutine in the plurality of subroutines, again transfers program execution control from the main routine to the first subroutine at the address of the decision point contained in the first multitasking vector, and wherein said main routine uses other multitasking vector to subsequently and sequentially transfer program execution control back to each remaining subroutine at an address of a decision point contained in each of the other multitasking vectors.

Kaneko teaches in Fig. 3 and in col. 5, line22 through col. 6, line 7, "Then, the subroutine SUBI beginning at address Y is called by instruction CALL BX in the bank switching control program in the second memory block 15, and it is executed. Upon completion of the execution of subroutine SUBI, the RET instruction transfers control back to the bank switching control program in the second memory block 15 so that the bank is switched from the second memory block 15 to the first memory block 14. Subsequently, the RET instruction of the bank switching control program in the first memory block 14 brings the process back to the main routine. (14) In calling the subroutine SUB2, address W is transferred to the register BX at address X of the main routine." Thus, Kaneko teaches" a plurality of subroutines sequentially callable by said main routine and wherein the main routine a after sequentially transferring program

execution control to each remaining subroutine in the plurality of subroutines, again transfers program execution control from the main routine to the first subroutine and wherein said main routine uses other multitasking vector to subsequently and sequentially transfer program execution control back to each remaining subroutine.

Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a network interface card with a microcontroller including multitasking control program comprising the main routine and a plurality of subroutines callable by main routine in the first memory as taught by Cooper and Johnson and providing multitasking vectors in the second memory associated with the multitasking control program where the status of the subroutines is updated periodically for coming back to check it's progress of execution because if one subroutine fails to terminate the microcontroller becomes incapable of executing any further instructions as taught by Cooper and enhancing by Kaneko' teachings such that every single subroutine is sequentially executed. This would have been obvious because this allows the use of a ROM of less capacity for the program memory as taught by Kaneko in col. 11, line 35-43.

Referring to claims 3, 4, 5 and 6,

Cooper teaches the first memory as being a read-only memory (ROM) (Fig.2, element 200), the second memory as being a random access memory (RAM) (Fig.2, element 202), and both, ROM and RAM memories are internal to the microcontroller (Fig.2). The reference also teaches ROM as being an external device coupled to microcontroller through secondary bus. (Fig. 1, elements 102, 134 and 124).

Referring to claims 7 and 8,

Cooper teaches that the components such as dispatch and watch dog timers can be incorporated within the microcontroller or be external to the microcontroller. It also teaches that a computer processor can also perform the methods performed by the microcontroller. It also teaches the various memory storage devices that may be used with a microcontroller. (col.5, lines 26-42). Thereby, it teaches that the first memory and second memory needed for storing and executing the microcontroller control program routines and subroutines (microcontroller firmware instructions, task initialization and service routines) may be RAM or ROM or a combination of both, which can be externally or internally coupled to a microcontroller.

Referring to claims 9 and 10,

Claims 9 and 10 are rejected for the reasons set forth for the claims 1 and 2, and Cooper's teaching of a processing system including a data processor. (Fig. 1 element 104).

Referring to claims 11, 12, 13 and 14,

Claims 11, 12, 13 and 14 are rejected for the reasons set forth for the claims 3, 4, 5 and 6.

Referring to claims 15 and 16,

Claims 15 and 16 are rejected for the reasons set forth for the claims 7 and 8.

Referring to claims 17 and 18,

Claims 17 and 18 are the methods of the claims 1 and 2. Therefore claims 17 and 18 are rejected for the reasons set forth for claims 1 and 2.

Referring to claims 19, 20, 21 and 22,

Claims 19, 20, 21 and 22 are the methods of the claims 3, 4, 5 and 6. Therefore claims 19, 20, 21 and 22 are rejected for the reasons set forth for claims 3, 4, 5 and 6.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A. Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abp
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